

CLAIMS

1. A method of powering a cold cathode fluorescent light (CCFL) circuit, the method including:

 determining a frequency provided to power the CCFL circuit based on a duty cycle of a driving waveform to the CCFL circuit.

2. The method of Claim 1, wherein the duty cycle of the driving waveform is approximately 50%.

3. The method of Claim 2, wherein determining the frequency includes sensing a voltage of the driving waveform at a first node.

4. The method of Claim 3, wherein determining the frequency further includes setting values of a plurality of resistors for sensing the voltage of the driving waveform.

5. The method of Claim 4, wherein setting values is dependent on a defined duty factor.

6. The method of Claim 4, wherein setting values is dependent on a high level of the driving waveform.

7. The method of Claim 4, wherein setting values is dependent on a set reference voltage.

8. The method of Claim 3, wherein determining a frequency includes generating a first DC signal that is proportional to a time-averaged voltage at the first node.

9. The method of Claim 8, further including:

sensing a voltage at a second node that is proportional to a CCFL current; and

generating a second DC signal that is proportional to a time-averaged voltage at the second node, wherein the second DC signal is used in determining the frequency.

10. The method of Claim 9, further including clamping the second DC signal.

11. The method of Claim 10, further including clamping the first DC signal.

12. The method of Claim 11, wherein clamping the first DC signal includes selecting one of a plurality of current sources.

13. The method of Claim 12, further including generating an interrupt signal that controls the driving waveform.

14. A system for powering a cold cathode fluorescent light (CCFL) circuit, the system including:

an output driver for generating a driving waveform to the CCFL circuit;

a first control loop connected to a first node that provides a first voltage proportional to a current through the CCFL circuit;

a first integrator for generating a first DC signal that is proportional to a time-averaged voltage at the first node;

a second control loop connected to a second node that provides a second voltage proportional to a voltage of the driving waveform;

a second integrator for generating a second DC signal that is proportional to a time-averaged voltage at the second node;

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a voltage controlled oscillator for receiving the second DC signal and generating a frequency signal; and

a comparator for receiving the frequency signal and the first DC signal and generating a pulse width modulated signal for the output driver.

15. The system of Claim 14, wherein the second integrator receives a reference voltage based on a duty factor of the driving waveform.

16. The system of Claim 15, wherein the duty factor is approximately 50%.

17. The system of Claim 15, wherein the duty factor is between approximately 40% and 50%.

18. The system of Claim 14, further including a first clamp connected to an output of the first integrator.

19. The system of Claim 18, wherein the first clamp is configured to allow the first DC signal to increase at a rate that is no faster than a first current source can charge a first capacitor.

20. The system of Claim 19, further including a second clamp connected to an output of the second integrator.

21. The system of Claim 20, wherein the second clamp is configured to allow the second DC signal to increase at a rate that is no faster than a second current source can charge a second capacitor.

22. The system of Claim 21, wherein the second clamp includes a plurality of current sources and a switch to select the second current source from the plurality of current sources.

23. The system of Claim 22, further including a ramp generator that outputs a first interrupt signal to the output driver, wherein the first interrupt signal turns the CCFL circuit off and on, thereby adjusting the brightness of the CCFL circuit.

24. The system of Claim 23, further including a third control loop connected to a third node that provides a voltage proportional to the voltage across the CCFL.

25. The system of Claim 24, wherein the third control loop includes fault logic that outputs a second interrupt signal to the output driver, wherein the second interrupt signal is longer than the first interrupt signal.

26. Clamping circuitry for a line, the clamping circuitry comprising:

a comparator including a positive input terminal, a negative input terminal, and an output terminal;

a transistor including a source connected to a predetermined voltage source, a gate connected to the output terminal of the comparator, and a drain connected to the positive input terminal of the comparator and the line;

a capacitor including a first terminal connected to the predetermined voltage source and a second terminal connected to the negative input terminal of the comparator;

at least one current source connected to the negative input terminal of the comparator; and

a reset switch connected to the negative input terminal of the comparator, wherein the reset switch selectively provides a path connected to the predetermined voltage source.

27. The clamping circuitry of Claim 26, wherein the predetermined voltage source is VSS.

28. The clamping circuitry of Claim 26, wherein the predetermined voltage source is ground.

29. The clamping circuitry of Claim 26, wherein the transistor is an n-type transistor.

30. The clamping circuitry of Claim 26, wherein the at least one current source includes a first current source and a second current source, and wherein the clamping circuitry further includes a current switch for selectively connecting one of the first current source and the second current source to the negative input terminal of the comparator.

31. A method for controlling a voltage increase on a line, the method including:

limiting the voltage increase to a first predetermined amount based on a first current source and a capacitor; and selectively resetting a capacitance of the capacitor to zero to provide a soft start on the line.

32. The method of Claim 31, further including switching to a second current source, thereby limiting the voltage increase to a second predetermined amount based on the second current source and the capacitor.

33. A high side driver for providing a drive signal to a CCFL circuit, the driver comprising:

a first pulse generator circuit for pulling the drive signal up to a first predetermined value during a first transition of an input signal to the driver;

a first current source circuit for maintaining the first predetermined value during a first state of the input signal;

a second pulse generator circuit for pulling the drive signal down to a second predetermined value during a second transition of the input signal; and

a second current source circuit for maintaining the second predetermined value during a second state of the input signal.

34. The driver of Claim 33, wherein at least one of the first pulse generator circuit, the first current source circuit, the second pulse generator circuit, and the second current source circuit includes an n-type transistor comprising a lightly doped drain.

35. The driver of Claim 33, wherein at least one of the first pulse generator circuit, the first current source circuit, the second pulse generator circuit, and the second current source circuit includes an p-type transistor coupled to a device with diode characteristics for protecting the p-type transistor.

36. The driver of Claim 33, wherein a plurality of transistors in the first pulse generator circuit, the first current source circuit, the second pulse generator circuit, and the second current source circuit receive a battery voltage on at least one of their terminals.

37. The driver of Claim 35, wherein the device with diode characteristics includes a clamp.

38. A method for providing a drive signal to a CCFL circuit, the method comprising:

generating a first pulsed signal for pulling the drive signal up to a first predetermined value during a first transition of an input signal to the driver;

using a first current source to maintain the first predetermined value during a first state of the input signal;

generating a second pulse for pulling the drive signal down to a second predetermined value during a second transition of the input signal; and

using a second current source circuit to maintain the second predetermined value during a second state of the input signal.

39. The method of Claim 38, further including limiting the second predetermined value by using a device with diode characteristics.